Research Activities on the Single-Chip Cloud Computer

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Contents

1 Introduction

This edition includes a summary of the major projects that have occupied the Single-Chip Cloud Computer (SCC) ranging from August 2011 up to March 2013. The SCC is an experimental processor created by Intel Labs. It is a 48-core "concept vehicle" created as a platform for many-core software research [7]. The purpose of the current edition is to familiarize any interested party with the work that has been performed at MicroLab using the aforementioned piece of hardware.

In the current report, we will not be delving into the technical details of the SCC's architecture and programming style. Any interested reader is encouraged to inspect related publications for in-depth understanding of this processor [7, 13]. However, we believe that a brief description is deemed necessary, at least to cover some key terminology: The SCC processor consists of 48 P54C cores that are interconnected with a high speed mesh network. The cores are organized in pairs called *tiles*. SCC cores feature a private memory space like typical systems. However, at the lowest level, a small memory bank is assigned to each core for the submission and retrieval of messages. This memory bank is called Message Passing Buffer (MPB) and enables inter-core communication.

The SCC chip is placed on a board that communicates with a standard server (Management Console Personal Computer – MCPC) through a PCIe cable. The MCPC is responsible for dispatching processes to user-defined cores through `pssh`. Parallel code is written on the MCPC, using functions of a message passing library, called RCCE (pronounced "rocky") [14]. This library enables synchronization between cores, message passing and dynamic frequency and voltage scaling [13].

Each of the following Sections is dedicated to a single research topic that occupied the SCC platform and has been authored by the responsible researcher in each case. Dissemination of the discussed topics to conferences or workshops is cited accordingly. The interested reader can follow these citations for further information about each topic. Alternatively, contacting the responsible researcher is also encouraged. At the end of each Section we list contact information for each researcher.

In the context of our work, the SCC infrastructure is used under the supervision of the Principal Investigator, Dr. Antonis Papanikolaou. The co-authors of this edition would like to thank Prof. Dimitrios Soudris from MicroLab-ECE-NTUA and Prof. Elias S. Manolakos from DIT-UOA, for their additional supervision. Finally, on behalf of all involved researchers, we would like to thank Dr. Xavier Vera and Mr. Enric Herrero of Intel Labs Barcelona for enabling use of the SCC; Intel Labs Braunschweig for providing the related hardware and the Intel MARC communities.

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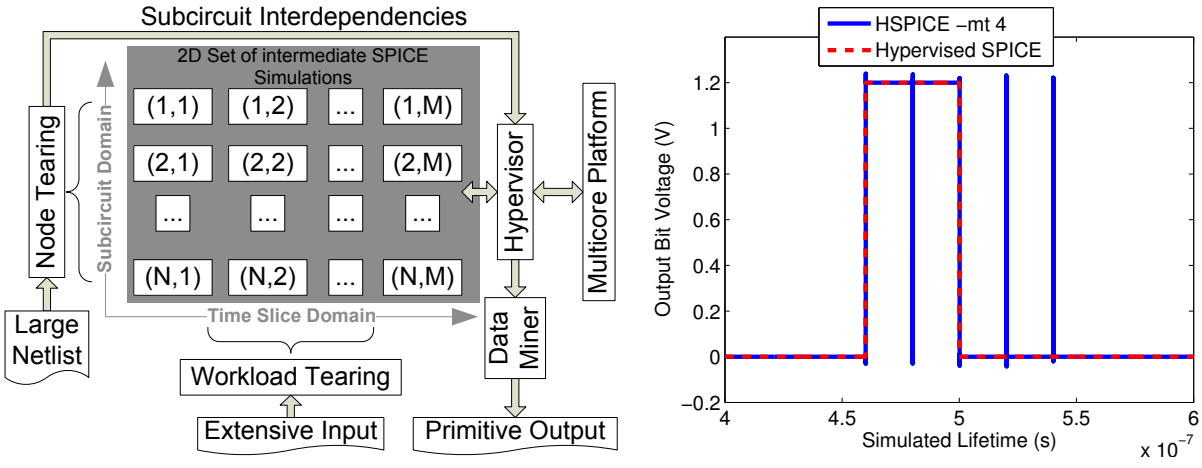
2 Hypervised SPICE for Massive Netlists and Workloads

Abstract: Advances in modern computer architecture have drastically pushed application development to parallel programming. Industry standard SPICE applications have also followed this trend and multi-threaded execution has led to significant advances in the field of circuit simulations limited only by the memory of the respective runtime systems. Therefore there is a need for flexible memory conservative and scalable techniques for parallel application development. This project attempts to attack this issue with the use of a versatile development framework applied in the field of circuit simulations. One of the platforms used to prove the versatility of the framework is the SCC.

Ever since the begining of circuit design there has been a need for circuit simulations. Nowadays digital circuits are an integral part of everyday life. Everything from smartphones to super computers depends on them. Therefore the need for detailed circuit simulations is at it's peak. The field of circuit simulations has constantly grown more computationally intensive over the years. What's more, modern reliability models require massive computational resources in order to complete the simulation.

In order to fill the need for fast and accurate simulations there are many approaches to the optimisation of SPICE applications . Single thread optimisations have been performed over the years on the SPICE kernels that run the simulations [15]. Since multithreaded execution has been introduced developers realised that parallel programming is a promising field and with the advances in modern processors it is only logical that SPICE applications would follow the trend and try to harness the new processing potential [16]. There have also been attempts to run SPICE on specialised hardware such as FPGAs [9] or GPUs [6] with promising results. Many steps have been taken and significant advances have been made, though little is done to minimise memory usage on large netlists and massive workloads, thus many simulations stop to a halt due to bad alloc errors [4].

This project attempts to attack the issue from a different angle. Instead of working in the SPICE kernel source code the framework uses a wrapper and remains agnostic regarding the executable code. In order to achieve that we adopt two methods of data partitioning *Workload* and *Node tearing* [12]. When it comes to input signals one can easily comprehend the concept of *Workload tearing* which consists of signal partitioning on the axis of time. What must be pointed out is that the partitioning method is sophisticated enough to ensure that the accuracy of the simulation is not compromised. On top of that we employ another method of data partitioning referenced as *Node tearing*. The initial netlist is broken down to components that have directed acyclic dependencies between them. The intermediate results are forwarded by the framework among the components. This is represented in a task graph parsed by the framework, enabling the distribution of the tasks described, over a set of execution nodes. Running the simulations independently minimizes the need for massive memory allocation requests thus allowing the simulations to complete.



(a) Framework concept

(b) Comparison of results

Figure 2.1: Framework concept and results comparison

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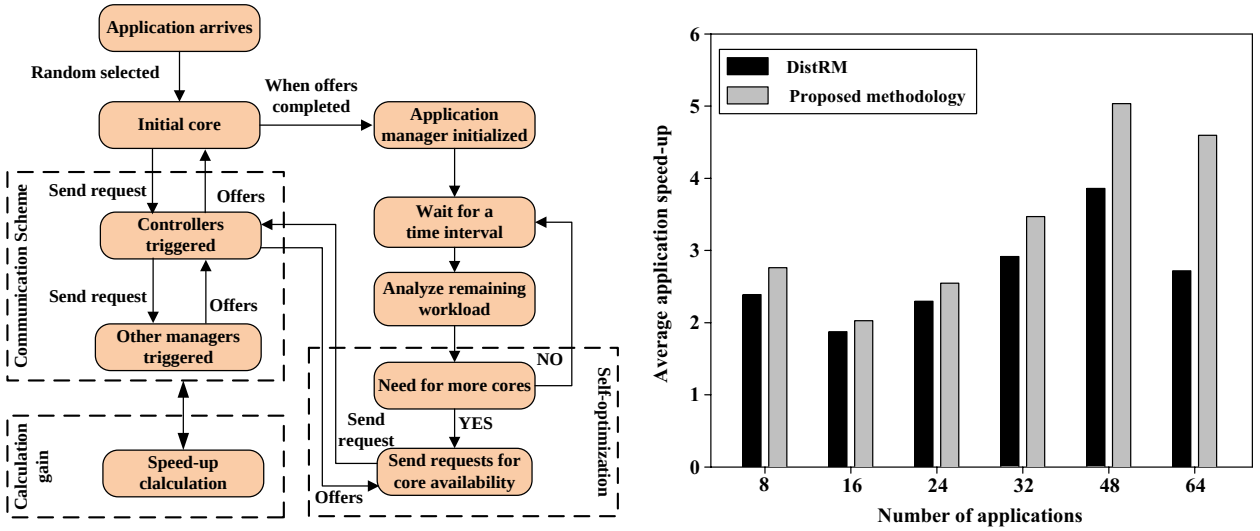

(a) Overall flow of the proposed methodology

(b) Average application speed-up using the speed-up function presented in [11]

Figure 3.2: Distributed Run-Time Resource Management on Single-Chip Cloud Computer (SCC)

3 Distributed Run-Time Resource Management

Abstract: Prevalent solutions for modern embedded systems and general computing employ many processing units connected by an on-chip network leaving behind complex superscalar architectures. Here, we couple the concept of distributed computing with parallel applications and present a workload-aware distributed run-time framework for malleable applications. The framework is responsible for serving in a distributed way and at runtime, the needs of malleable applications, maximizing resource utilization avoiding dominating effects and taking into account the type of processors supporting platform heterogeneity, while having a small overhead in overall inter-core communication. The framework has been implemented as a run-time service on the SCC and has been compared against a state-of-art run-time resource manager. Experimental results showed that our framework has on average 70% less messages, 64% smaller message size and 20% application speed-up gain.

The run-time resource management paradigm has been revealed as a key challenge to modern multi-core systems and it has become prominent due to the run-time dynamism of modern parallel applications and platforms. In large-scale execution environments such as multi-cluster systems and grids, resource availability may vary due to resource failures and because resources may be added to or withdrawn from such environments at any time thus making the resource allocation problem significant to the overall system performance. In addition, dedicated resources or fixed resource allocation strategies fail to provide the desired high performance that applications expect from large pools of resources.

In this work, we couple the concept of distributed computing with parallel applications and we present a workload-aware distributed run-time framework for malleable applications running on many-core platforms. The proposed framework is based on the idea of local controllers and managers while an on-chip intercommunication scheme ensures decision distribution. The presented framework is responsible (i) for serving, at run-time, the needs of malleable applications, in terms of processing cores; (ii) makes sure that the application will get the optimum number of cores avoiding dominating effects; (iii) it takes into account the type of processors best utilizing any platform's heterogeneity; and (iv) it has a small overhead in overall core intercommunication.

Figure 3.2b presents the average application speed-up using the speed-up function presented in [11]. Speed-up is defined as the ratio of the total number of turnarounds performed for all applications divided by the total workload. The presented framework achieves on average 20% better application speed-up than DistRM. This can be explained by the fact that in the presented framework cores are not disturbed so often by messages during their application execution and thus completing the applications faster. On the other hand, due to the large number of messages sent by the application agents in DistRM, cores stop their functionality more frequently in order to answer to these messages, thus delaying the execution.

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4 SDC Mitigation on SCC Streaming Applications

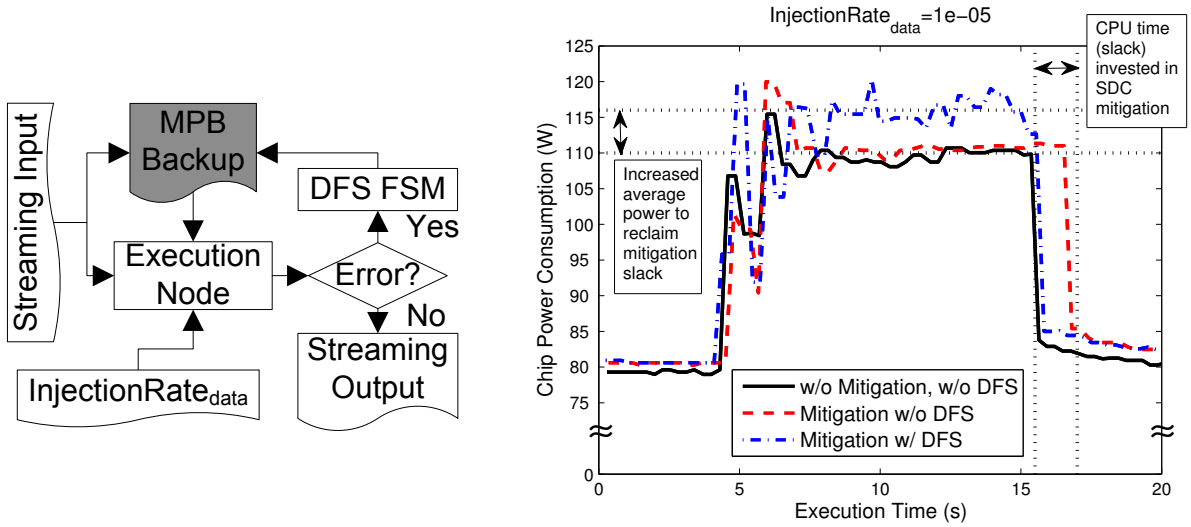
Abstract: This work presents a hybrid HW-SW mitigation scheme against Silent Data Corruptions (SDCs) on the SCC platform. The methodology assumes *error detection* implemented in hardware (HW). Also, the MPBs of each core are assumed to implement both *error detection and mitigation* in HW. Upon error detection, a software (SW) rollback is triggered, while retrieving error-free copies of corrupt data from the closest MPB. Given the context of streaming applications, the processing time invested in mitigation needs to be reclaimed. The dynamic frequency scaling utilities of the target platform are used to reclaim that slack, depending on the level of SDC aggression.

A usual distinction between erroneous states found in digital systems is between permanent and transient errors [22]. We focus on the latter category, namely the corruption of the logic state of a circuit node because of an intermittent phenomenon. Typical examples of such errors are Single- or Multiple-Event Upsets caused by cosmic particles or erroneous logic states due to IR-drops in the power or ground grid of the platform [24]. In the past, transient errors of that sort where exclusively mitigated in HW. However, with decreasing device dimensions, the mitigation overhead purely in HW is becoming too extreme [10].

Our focus is narrowed down to SDCs, which affect the data plane of the target system, without altering the control flow of the executing application. SDCs are injected at runtime in the application's data plane. The intensity of SDCs is abstracted by the $\text{InjectionRate}_{\text{data}}$ metric, representing the probability of a data plane bit being flipped [17]. Assuming binary corruption of separate bits as independent events, we can calculate the probability for a streaming data structure to be corrupt.

The target application of this work is a data-parallelized MJPEG decoder. A single frame decoder [20] occupies a triplet of SCC cores (execution nodes), hence we end up with 16 JPEG decoders decoding in parallel the frames of an MJPEG video benchmark. This being a streaming application, we can identify the data required by each execution node of each decoder instance. An error-free copy of each key data structure is kept in the local MPB once the former is created. That way, assuming that the MPB is HW-protected against transient errors, we can retrieve the error-free copy upon error detection. This retrieval is SW-controlled, by altering the source code of the streaming application (see Figures 4.3a).

Even if demand driven, the SW rollbacks are consuming processing time. Especially in case of increased $\text{InjectionRate}_{\text{data}}$ values, we need to reclaim the processing time invested in mitigation, in order not to affect application performance. We use the Dynamic Frequency Scaling (DFS) of the chip to accelerate a portion of the execution, in order to meet the specification about decoded frames per second. Temporarily increasing the frequency, comes with a power consumption penalty, as illustrated in Figure 4.3b. We have explored the average power impact that slack reclaiming with DFS has under different $\text{InjectionRate}_{\text{data}}$ [18]. Absorbing mitigation overhead using DFS is upper bounded by the highest frequency that the SCC cores can achieve.



(a) Simplified flowchart of the SW-enabled rollbacks upon SDC detection

(b) Impact of reclaiming slack with DFS on the transient power of the SCC: the temporal overhead translates to increased average power

Figure 4.3: Concept and transient power trace for the proposed HW-SW SDC mitigation technique

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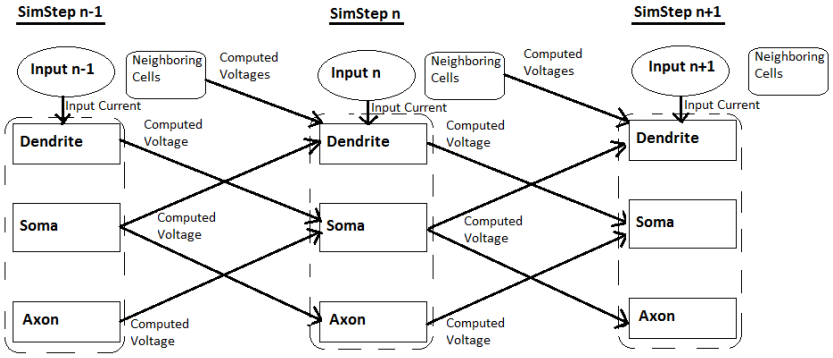

Figure 5.4: Data flow and communication between cells and compartments of the target cell

5 Scalable Simulation of the Inferior Olivary Nucleus

Abstract: This work contains a model of the inferior olive brain cells network, an important subsystem for the functionality of the cerebellum, as depicted in a mesh, with varying network size and level of interconnectivity between the cells. The cell model is comprised of 3 functional units (compartments), representing the dendrite, soma and axon parts of the biological neuron. These units should be mapped to SCC tiles accordingly and communicate with each other. The network is organized as a typical mesh. Using outside stimuli and the previous cell states as input parameters, the voltage output of each cell compartment is computed. Communication and computational costs are prohibitive of simulating large, complicated networks so far, thus efforts to increase simulation speed is of great value.

The human brain processes data in a very different way than typical man-made computing systems. Brain cells process data using the propagation of spikes between a network of neuron cells. Information is encoded in the spikes' frequency, amplitude and shape pattern. The exact details of these mechanisms are still heavily debated [23]. The cerebellum has the greatest concentration of neurons in the brain and is imperative for motor learning and synchronization of body movement. In particular, the inferior olive cerebellum subsystem is of great importance in such functions and, thus, a major subject of scientific debate [3]. An application simulating the voltage levels of the olive cells is highly valued and needed, as well as computationally taxing. The porting of a scalable model [1, 8] on a high-computational capacity platform as the SCC is described below.

The inferior olive cells are represented in a mesh of variable dimensions where each element is a cell of the three compartments(or compartments in neuroscience), the soma, the axon and the dendrite. Each mesh element can be fed by an input current as external stimulus. As shown in Figure 5.4, the dendrite is the compartment that operates as the cell input. It models connectivity between neighboring cells (by receiving voltage inputs from other cells) and is fed the previous cell state and external input stimuli. The compartments of a single cell also communicate with each other (some voltage level). After information of the previous step (soma voltages) is gathered and input of the current step is stored in a buffer, the compartment computes all relevant parameters to store their new state and the simulation advances for as many steps as indicated by the simulation process. The voltage outputs of each cell for every simulation step are recorded in an output file.

Currently the output evoked by the input stimuli is a certain kind of spike typical of the IO cell (complex spike) that triggers once at a particular time period. The input current values are hard-coded and the correct response values are recorded and compared against a reference output. However, a possible extension of the work will incorporate different input stimuli completely controlled by the user of the application so as to provide more feedback on the behavior of the simulated inferior olive cells. Furthermore, communication between the cells is restricted to immediate neighbors. Higher degrees of interconnectivity can be pursued to replicate real-life cell communication, which will greatly increase the value of the application. In such case, the increase in communication cost needs to be weighed. Thus the computational capacities of the SCC will be greatly tested and exploited, even more than by simply increasing the mesh size.

Since the soma compartment has workload roughly equal to the sum of the dendritic and axonal workloads, the project plans on using SCC tiles: one core handles soma computation and the other one is assigned the dendrite and axon compartments. This will also exploit the locality of two cores belonging to one tile. However, since the dendritic compartment is responsible for communicating with neighboring cells and registering incoming stimuli, if greater amount of inter-connectivity between cells is pursued, the dendrite may exhibit greater workload than the soma and different porting patterns will be explored.

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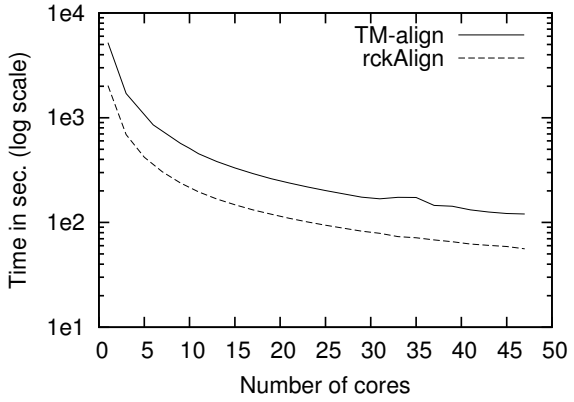
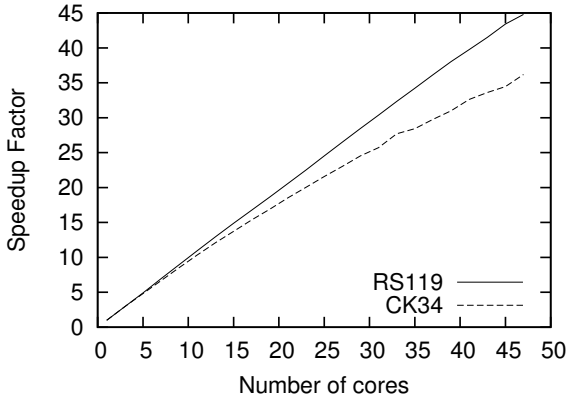


(a) Performance comparison of parallel *rckAlign* with that of distributed TM-align software (C port) for the Chew-Kedem dataset as the number of slave cores used is increasing.



(b) Speedup achieved by *rckAlign* as the number of slave cores is increasing (from 1 to 47) for the Chew-Kedem (CK34) and the Rost-Sanders (RS119) datasets.

Figure 6.5: Performance comparison and speedup achieved by SCC port of TM-align

6 Protein Structure Comparison on Many-Core NoCs

Abstract: This work presents *rckAlign*, an implementation of the popularly used TM-align PSC algorithm, designed for the Single-Chip Cloud Computer (SCC). We developed a skeleton library, *rckskel*, and implemented a master-slaves variant of TM-align to exploit the parallelism offered by the SCC. We observed a 44-fold speedup relatively to a single-core of the SCC. A key aspect of the performance of *rckAlign*, is the almost linear speedup achieved with the number of SCC cores used as slaves. The method presented can easily be applied to other PSC algorithms and extended to running multiple PSC algorithms within the same SCC chip.

A typical task in bioinformatics is comparison of the structure of a protein with a database of known protein structures, one-to-many protein structure comparison (PSC), or when a set of multiple proteins is of interest, comparison of their structures to a whole database of known protein structures, many-to-many PSC. The unit operation in both these forms of PSC is the comparison of structures of a pair of proteins [21]. Computational demand of the one-to-many and many-to-many PSC problem are a result of factors such as: exponential growth of structural proteomics databases, pairwise protein structure comparison is computationally intensive and several pairwise comparison approaches are typically of interest to the researcher [2].

Algorithmic skeletons [5] allow a programmer to develop algorithms without specifying architecture dependent details. By nesting and combining skeletons desired level of parallelism can be introduced into different PSC methods. Using algorithmic skeletons allows programs to fully exploit the parallelism afforded by many-core processor architectures, while retaining the flexibility needed for experimenting with the level of parallelism and shared tasks (such as rotation of structures).

In order to facilitate development of PSC algorithms targeted for the SCC, we built a C library. The library we built is a small parallel programming library which implements algorithmic skeletons - *SEQ, PIPE, MAP, FARM* - in addition to providing convenient wrappers for common RCCE related tasks. Allocation of a core to a job is performed dynamically by the library, based on the number of jobs and the number of cores available for processing. A master-slaves implementation of the C code of TM-align, was developed using the *FARM* skeleton of the *rckskel* library [19].

As shown in Figure 6.5a faster processing times are achieved by *rckAlign* as compared to the distributed port, where a master process is running on the MCPC. There are two main reasons for this behavior: (a) disk access through the Network File System (NFS) creates a bottleneck when multiple processes are trying to access the data, and (b) high environment setup costs incurred while issuing remote processing.

As can be seen in Figure 6.5b an almost linear speedup is achieved by the master-slaves port of TM-align. We also observed that the larger the dataset the higher the speedup observed. These results suggest that many-core NoCs with fast interconnection networks and faster processor cores than the SCC will be ideal candidates for delivering high performance for all-to-all PSC tasks applied to large size protein databases, as needed for combinatorial drug design.

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